# A MINIATURIZED, BROADBAND MMIC FREQUENCY DOUBLER

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## Abstract

**A miniaturized, broadband balanced MMIC frequency doubler, which consists of a common gate FET and a common source FET directly connected to each drain electrode, is proposed. A chip size of 0.5 mm × 0.5 mm is achieved excluding the output matching circuit with conversion loss less than 9 dB, fundamental signal suppression better than 18 dB, and input return loss better than 8 dB from 6 GHz to 16 GHz.**

## Introduction

Frequency doublers and multipliers are important circuits in microwave components. Recently, single-ended frequency doublers[1], and balanced frequency doublers[2] which consist of two single-ended doublers and a balan for balanced operation, have been demonstrated in the monolithic form. Another wide-band frequency multiplier[3], which employs distributed amplifier architecture, has been reported. However, the conventional doublers need large chip size because the doublers require large quarter-wavelength transmission lines for fundamental frequency trapping, hybrids and balans. The distributed amplifier configuration also requires large chip size due to use of several FETs and many inductive lines.

In this paper, a miniaturized, broadband balanced MMIC frequency doubler is proposed. The doubler consists of a common gate FET (CGF) and a common source FET (CSF) connected in series at source-gate-drain-gate-source electrode locations. An advantage of the proposed doubler is that it remarkably reduces MMIC chip size, as well as operates in broad band, due to an active trapping of fundamental signals between the CGF and CSF, and an active input impedance match by CGF. The MMIC chip size is as small as $0.5mm \times 0.5mm$.

*ATR: *Advanced Telecommunications Research Institute International*

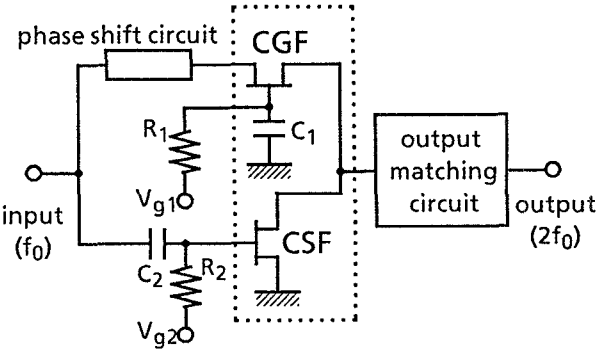


Fig. 1. A proposed frequency doubler configuration.

## Configuration

The configuration of the proposed balanced frequency doubler is shown in Fig. 1. The doubler consists of a common gate FET (CGF) and a common source FET (CSF) connected in parallel electrically and in series at electrode locations, that is, source-gate-drain-gate-source. A second harmonic output matching circuit and a phase shift circuit compensating for phase error between outputs from the CGF and CSF are added to the CGF, CSF configuration, where

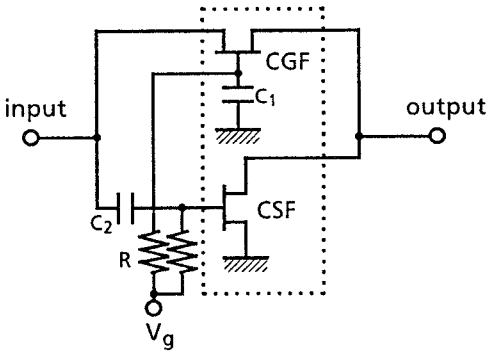


Fig. 2. A simplified frequency doubler configuration.

no input matching circuit is required because of the active matching effect of the CGF.

Figure 2 shows a simplified frequency doubler which has a configuration similar to that in Fig. 1. The doubler is constructed with only a CGF, CSF and dc bias circuit. This configuration offers a doubler module for generic use. The simplified doubler in Fig. 2 is, in this paper, designed and demonstrated.

The doubler operates near the gate-source pinch-off voltage which is given through the gate resistors and capacitors. The drain currents through CSF and CGF are swung by each input signal level. Amplitudes of output signals from the two FETs are made equal by adjusting each gate bias. In the CSF section, output phase shifts at the fundamental frequency and second harmonic are 180 degrees and 360 degrees, respectively. In the CGF section, the output phase shifts at the fundamental frequency and second harmonic are the same, 0 degrees. Thus, the fundamental frequency signals from the CGF and CSF cancel each other. On the other hand, the second harmonics are emphasized. This active trapping and the input active match realize a miniature broadband doubler.

## Design

In order to determine the gate width of the FETs, a harmonic balance nonlinear circuit simulation was performed.

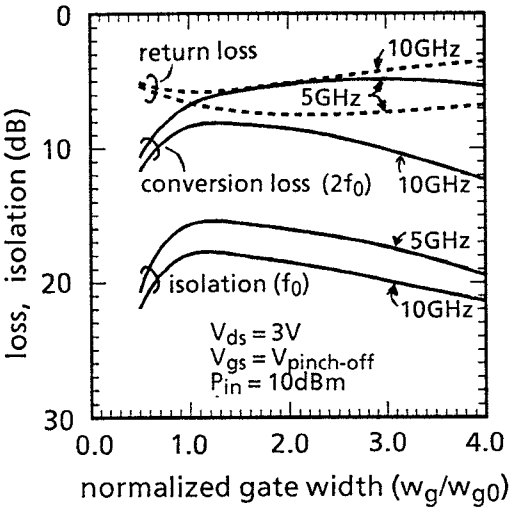


Fig. 3. Characteristic of the doubler vs. gate width of FETs. (input frequency $f_0$ : 5GHz, 10GHz)

Calculated characteristics of the doubler, dc biased at gate-source pinch-off voltage, are shown in Fig. 3. Input power is 10 dBm. The CGF and CSF of the module have the same gate width $w_g$, in the estimation, and $w_g$ is normalized by the gate width $w_{g0}$ of the CGF in the small-signal active matching condition, that is $g_m Z_0 = 1$, where $g_m$ and $Z_0$ are the transconductance of the CGF and input port impedance, respectively.

The difference between the conversion loss at 5 GHz and 10 GHz expands considerably above the $w_g/w_{g0}$ value of 2. Therefore, gate width $w_g$ less than $2w_{g0}$ is required for broadband frequency-multiplying, as well as for lower conversion loss, as shown in the figure. Fundamental frequency suppression, isolation, is better than 15 dB at each $w_g/w_{g0}$ value, and is gradually improved as the $w_g/w_{g0}$ value increases. Input return loss is maximum at a $w_g/w_{g0}$ value between 1 and 3. As a result, a gate width $w_g$ of between $w_{g0}$ and $2w_{g0}$ is chosen in the design, and the gate-source dc bias voltage is adjusted for better performance in practical operation.

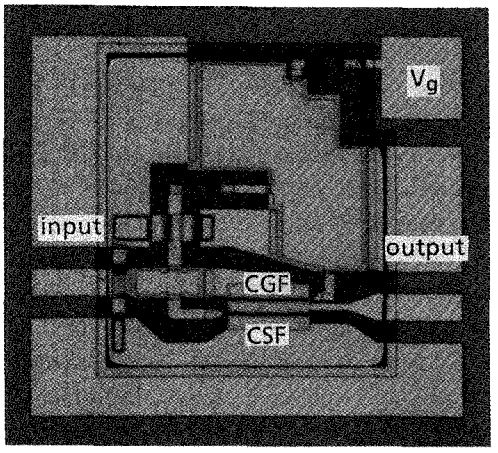


Fig. 4. Photomicrograph of the fabricated MMIC doubler. (chip size: $0.8mm \times 0.7mm$, intrinsic : $0.5mm \times 0.5mm$)

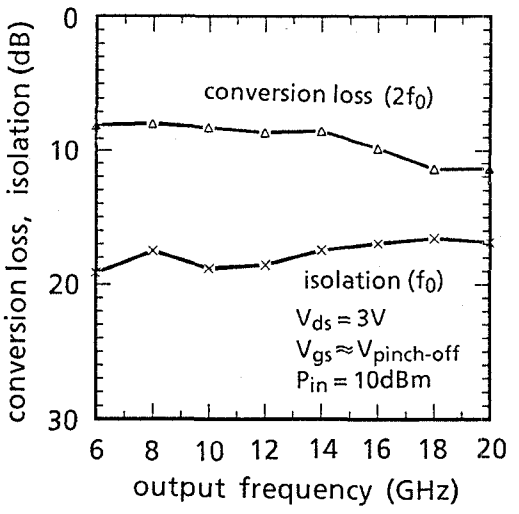


Fig. 5. Conversion loss and isolation of the doubler.

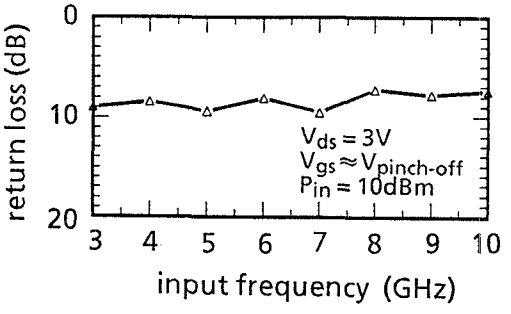


Fig. 6. Input return loss of the doubler.

### Experiment results

An MMIC frequency doubler implemented using the conventional GaAs MMIC process, is shown in Fig. 4. The input and output coplanar waveguide impedance is $50\Omega$ for on-wafer measurement. The chip size is $0.8mm \times 0.7mm$, and the intrinsic area is only $0.5mm \times 0.5mm$. This area is about 1/10 that of the previously reported doublers[1]. Ion implanted FET with a typical cutoff frequency of 20 GHz, $0.5\mu m$ gate length, and $150\mu m$ gate width are used in the doubler MMIC, where a gate width ratio $w_g/w_{g0}$ of 1.5 is employed according to the design.

The measured frequency response at 10 dBm input power is shown in Figures 5 and 6. The gate source voltage $V_{gs}$ is adjusted so that the MMIC exhibits input return loss around 10 dB and reasonably low conversion loss and high isolation, where $V_{gs}$ is $0.9V_p$ for CGF and $V_p$ for CSF. A conversion loss of 8 dB is achieved in the output frequency range from 6 GHz to 16 GHz. Fundamental frequency isolation is better than 17 dB up to 20 GHz. An input return loss better than 8 dB is achieved without any input matching circuits due to the active matching characteristic of the CGF. Power consumption is about 42 mW when the input signal power is 10 dBm. Degradation of the conversion loss at the output frequency between 16 GHz and 20 GHz is due to the absence of a phase compensation circuit. The operation frequency range is extended as the FET are improved and by using a miniature, thin film microstrip (TFMS) line phase shift circuit[4]. The broadband performance and very small size of the MMIC above are extremely valuable for generic use.

The measured performance as a function of 5 GHz input power is shown in Fig. 7. Conversion loss decreases gradually as the input power increases and approaches the minimum value of 8 dB above 10 dBm input power. Input return loss is improved monotonically and is better than 10 dB at an input power greater than 10 dBm. The fundamental frequency isolation is greater than 17 dB up to 15 dBm input power.

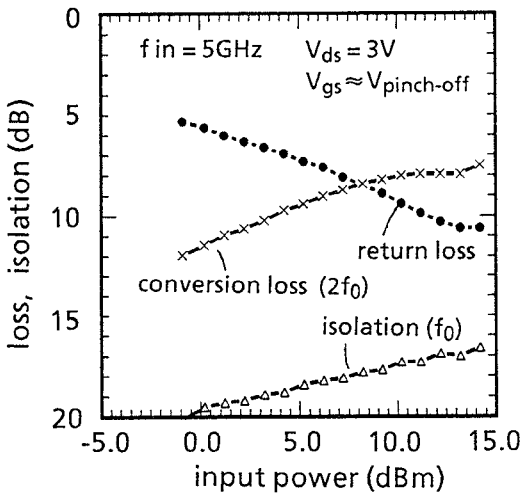


Fig. 7. Characteristic of the doubler vs. input power level.

## Conclusion

A miniaturized, broadband balanced MMIC frequency doubler, composed of a common gate FET and a common source FET directly connected to each drain electrode, has been proposed and demonstrated. The doubler is designed and fabricated as a function module. The chip size is only $0.5mm \times 0.5mm$, which area is about 1/10 that of the previously reported doublers. A conversion loss of 8 dB, a fundamental frequency suppression better than 17 dB, and an input return loss better than 8 dB are obtained in the output frequency range from 6GHz to 16GHz. The broadband doubler as a miniaturized MMIC function module can be applicable to small-size oscillator MMICs and multifunction MMICs.

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## Reference

[1] T. Ohira, T. Tokumitsu, T. Hiraoka, Y. Kihata, K. Araki, and H. Kato., "Development of key monolithic circuits to *Ka*-band full MMIC receivers", in *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.*, June 1987, pp.69-74.

[2] T. Hirota, and H.Ogawa, "Uniplanar monolithic frequency doublers", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-37, pp.1249-1254, August 1989.

[3] A. M. Patio, S. D. Bingham, R. H. Halladay, and C. A. Sapashe, "A distributed broadband monolithic frequency multiplier ", *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1988, pp.503-504.

[4] T.Hiraoka, T.Tokumitsu, and M.Aikawa, "Very Small Wide-Band MMIC Magic T's Using Microstrip Lines on a Thin Dielectric Film", *IEEE Trans. Microwave Theory and Techn.*, Vol.MTT-37, pp. 1569-1575, October, 1989.